WHAT IS CLAIMED IS:

1. A capacitive load driving circuit for supplying a charging-current to a capacitive load and withdrawing a discharging-current from said capacitive load, comprising:

an output circuit which comprises a power supply terminal, a ground terminal, and an output terminal connected to said capacitive load, and which performs a charging-current supplying operation of supplying a charging-current from said power supply terminal to said capacitive load and a discharging-current withdrawing operation of withdrawing a discharging-current from said capacitive load to said ground terminal; and

an overcurrent protection circuit for detecting a short circuit between said output terminal and said ground terminal so as to stop or suppress said charging-current supplying operation, and for detecting a short circuit between said output terminal and said power supply terminal so as to stop or suppress said discharging-current withdrawing operation; wherein

said output circuit selects any one of said charging-current supplying operation and said discharging-current withdrawing operation depending on the state of a control input signal.

2. A capacitive load driving circuit according to Claim 1, wherein said output circuit continues to charge said capacitive load in said charging-current supplying operation until the electric potential of said capacitive load reaches

a predetermined upper amplitude limit lower than the electric potential of said power supply terminal, and continues to discharge said capacitive load in said discharging-current withdrawing operation until the electric potential of said capacitive load reaches a predetermined lower amplitude limit higher than the electric potential of said ground terminal.

3. A capacitive load driving circuit according to Claim 1, wherein

said output circuit comprises: a first NPN transistor the collector of which is connected to said power supply terminal and the emitter of which is connected to said output terminal; and a first PNP transistor the collector of which is connected to said ground terminal and the emitter of which is connected to said output terminal; and wherein

said overcurrent protection circuit comprises: a second NPN transistor the collector of which is connected to the base of said first NPN transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a first voltage supply for generating a predetermined electric potential higher than the electric potential of said ground terminal; and a second PNP transistor the collector of which is connected to the base of said first PNP transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a second voltage supply for generating a predetermined electric potential lower than the

electric potential of said power supply terminal.

4. A capacitive load driving circuit according to Claim 2, wherein

said output circuit comprises: a first NPN transistor the collector of which is connected to said power supply terminal and the emitter of which is connected to said output terminal; and a first PNP transistor the collector of which is connected to said ground terminal and the emitter of which is connected to said output terminal; and wherein

said overcurrent protection circuit comprises: a second NPN transistor the collector of which is connected to the base of said first NPN transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a first voltage supply for generating a predetermined electric potential that is higher than the electric potential of said ground terminal and lower than or equal to said lower amplitude limit; and a second PNP transistor the collector of which is connected to the base of said first PNP transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a second voltage supply for generating a predetermined electric potential that is lower than the electric potential of said power supply terminal and higher than or equal to said upper amplitude limit.

5. A capacitive load driving circuit according to Claim 1, wherein the state of said control input signal alternates

periodically.

6. A capacitive load driving circuit for supplying a charging-current to a capacitive load and withdrawing a discharging-current from said capacitive load, comprising:

an output circuit which comprises a power supply terminal, a ground terminal, and an output terminal connected to said capacitive load, and which performs a charging-current supplying operation of supplying a charging-current from said power supply terminal to said capacitive load and a discharging-current withdrawing operation of withdrawing a discharging-current from said capacitive load to said ground terminal;

a current generation circuit for selecting, depending on the state of a control input signal, any one of a first state where a first current is supplied to said output circuit so as to cause said output circuit to select said charging-current supplying operation and a second state where a second current is supplied to said output circuit so as to cause said output circuit to select said discharging-current withdrawing operation;

a charging and discharging control circuit for detecting the electric potential of said capacitive load and thereby controlling and causing said output circuit to continue said charging-current supplying operation until the electric potential of said capacitive load reaches a predetermined upper amplitude limit, to stop said charging-current supplying

operation when said electric potential reaches said predetermined upper amplitude limit, to continue said discharging-current withdrawing operation until the electric potential of said capacitive load reaches a predetermined lower amplitude limit, and to stop said discharging-current withdrawing operation when said electric potential reaches said predetermined lower amplitude limit; and

an overcurrent protection circuit for detecting a short circuit between said output terminal and said ground terminal so as to stop or suppress said charging-current supplying operation, and for detecting a short circuit between said output terminal and said power supply terminal so as to stop or suppress said discharging-current withdrawing operation.

7. A capacitive load driving circuit according to Claim 6, wherein

said output circuit comprises: a first NPN transistor the collector of which is connected to said power supply terminal and the emitter of which is connected to said output terminal; and a first PNP transistor the collector of which is connected to said ground terminal and the emitter of which is connected to said output terminal; wherein

said overcurrent protection circuit comprises: a second NPN transistor the collector of which is connected to the base of said first NPN transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected

to a first voltage supply for generating a predetermined electric potential that is higher than the electric potential of said ground terminal and lower than or equal to said lower amplitude limit; and a second PNP transistor the collector of which is connected to the base of said first PNP transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a second voltage supply for generating a predetermined electric potential that is lower than the electric potential of said power supply terminal and higher than or equal to said upper amplitude limit; and wherein

said charging and discharging control circuit controls the base currents of said first NPN transistor and said first PNP transistor, so as to control the execution and the stop of said charging-current supplying operation and said discharging-current withdrawing operation.

8. A capacitive load driving circuit according to Claim 7, wherein said charging and discharging control circuit comprises: a third voltage supply for generating an electric potential equal to said upper amplitude limit; a fourth voltage supply for generating an electric potential equal to said lower amplitude limit; a charging control differential switch circuit one input terminal of which receives the electric potential of said capacitive load, and the other input terminal of which receives the electric potential of said third voltage supply; and a discharging control differ ntial switch circuit one input

terminal of which receives the electric potential of said capacitive load, and the other input terminal of which receives the electric potential of said fourth voltage supply; and wherein said charging control differential switch circuit performs on-off control of the base current of said first NPN transistor depending on the result of comparison between the electric potential of said capacitive load and the electric potential of said third voltage supply, while said discharging control differential switch circuit performs on-off control of the base current of said first PNP transistor depending on the result of comparison between the electric potential of said capacitive load and the electric potential of said fourth voltage supply.

9. A capacitive load driving circuit according to Claim 8, wherein the electric potentials of said third and fourth voltage supplies are variable, and wherein the electric potential of said first voltage supply varies in linkage with the electric potential of said fourth voltage supply, while the electric potential of said second voltage supply varies in linkage with the electric potential of said third voltage supply.

10. A capacitive load driving circuit according to Claim 8, wherein the electric potential of said first voltage supply is equal to the electric potential of said fourth voltage supply, while the electric potential of said second voltage supply is equal to the electric potential of said third voltage supply.

11. A capacitive load driving circuit according to Claim 6, wherein a frequency-dependent impedance element is provided between said current generation circuit and said output circuit, so that a part of the output current of said output circuit is fed back through said frequency-dependent impedance element to said current generation circuit, so that the through-rate is suppressed at the alternation of the output state of said current generation circuit.

12. A capacitive load driving circuit according to Claim 6, wherein the state of said control input signal alternates periodically.

13. A liquid crystal display comprising:

a liquid crystal display panel common electrode;

an output circuit which comprises a power supply terminal, a ground terminal, and an output terminal connected to said liquid crystal display panel common electrode, and which performs a charging-current supplying operation of supplying a charging-current from said power supply terminal to said liquid crystal display panel common electrode and a discharging-current withdrawing operation of withdrawing a discharging-current from said liquid crystal display panel common electrode to said ground terminal; and

an overcurrent protection circuit for detecting a short circuit between said output terminal and said ground terminal so as to stop or suppress said charging-current supplying

operation, and for detecting a short circuit between said output terminal and said power supply terminal so as to stop or suppress said discharging-current withdrawing operation; wherein

said output circuit selects any one of said charging-current supplying operation and said discharging-current withdrawing operation depending on the state of a control input signal.

14. A liquid crystal display comprising:

a liquid crystal display panel common electrode;

an output circuit which comprises a power supply terminal, a ground terminal, and an output terminal connected to said liquid crystal display panel common electrode, and which performs a charging-current supplying operation of supplying a charging-current from said power supply terminal to said liquid crystal display panel common electrode and a discharging-current withdrawing operation of withdrawing a discharging-current from said liquid crystal display panel common electrode to said ground terminal;

a current generation circuit for selecting, depending on the state of a control input signal, any one of a first state where a first current is supplied to said output circuit so as to cause said output circuit to select said charging-current supplying operation and a second state wh re a second current is supplied to said output circuit so as to cause said output

circuit to select said discharging-current withdrawing operation;

a charging and discharging control circuit for detecting the electric potential of said liquid crystal display panel common electrode and thereby controlling and causing said output circuit to continue said charging-current supplying operation until the electric potential of said liquid crystal display panel common electrode reaches a predetermined upper amplitude limit, to stop said charging-current supplying operation when said electric potential reaches said predetermined upper amplitude limit, to continue said discharging-current withdrawing operation until the electric potential of said liquid crystal display panel common electrode reaches a predetermined lower amplitude limit, and to stop said discharging-current withdrawing operation when said electric potential reaches said predetermined lower amplitude limit; and

an overcurrent protection circuit for detecting a short circuit between said output terminal and said ground terminal so as to stop or suppress said charging-current supplying operation, and for detecting a short circuit between said output terminal and said power supply terminal so as to stop or suppress said discharging-current withdrawing operation.